REMARKS

Claims 19-23, 73-76, and 83-92 are pending in this application. Claims 19, 73, 83, and 88 are independent.

The examiner objected to the drawings under 37 C.F.R. §1.83(a) on the ground that the provisions of 37 C.F.R. §1.83(a) require that the drawings show every feature of the invention specified in the claims, and that therefore the subject matter of claims 19, 73, 83, and 88 must be shown in the drawings, or the feature(s) cancelled from the claims.

Applicant traverses the examiner's objections to the drawings under 37 C.F.R. §1.83(a). Applicant contends that applicant's figures comply with 37 C.F.R. §1.83(a).

35 U.S.C. §113 states "[t]he applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented." Further, as provided by 37 C.F.R. §1.81(a), "[t]he applicant for a patent is required to furnish a drawing of his or her invention where necessary for the understanding of the subject matter sought to be patented."

Thus, the statutory provisions of the Patent Act regarding drawings, as well as rule 1.81(a), make it clear that it is not necessary to show in the drawings every feature of the claims as specified in the claims. Rather, it is only when the subject matter in the claims cannot be understood without the assistance of drawings that drawings become necessary.

Additionally, in discussing the requirements of 37 C.F.R. §1.83(a), MPEP 608.02(d) notes "[a]ny structural detail that is sufficient importance to be described should be shown in the drawings" (emphasis added). Thus, the Patent Office's own interpretation of the provisions of 37 C.F.R. §1.83(a) makes it clear that furnishing drawings corresponding to the features in the claims is not a mandatory requirement (as indicated by the use of the discretionary language "should be shown" in MPEP 608.02(d)).

Nevertheless, the drawings comply with 37 C.F.R. §1.83(a). Independent claim 19 is directed to a method executed in a processor. FIG. 1 shows a processor. The method includes loading a plurality of groups of bits from a source into a destination register, and duplicating the groups of bits in the destination register. The details of the elements of claim 19 are sufficiently clear that they can be understood without the use of drawings. Applicant also notes that pages 16, line 13, to page 21, line 2, of the originally filed application provide comprehensive

examples of embodiments of applicant's method, including visual illustrations of the operation of applicant's method. For example, in discussing applicant's MOVSLDUP instruction, the detailed description states at page 19, lines 15-17, "[s]pecifically, with a source being 3/2/1/0 (0 being the lower single-precision entry), a result register will store entries 2/2/0/0." Applicant, therefore, submits that it is not necessary, in this case, to have a drawing illustrating the features of independent claim 19.

Independent claims 73, 83, and 88, which recite features similar to those recited in independent claim 19, can likewise be understood without drawings.

The examiner rejected claims 19, 20, 22, 83, 84, 86, 88, 89, and 91 under 35 U.S.C. §102(b) as being anticipated by European Patent Application No. EP 0 743 594 A1 to Sidwell et al. The examiner also rejected claims 21, 23, 73-76, 85, 87, 90 and 92 under 35 U.S.C. §103(a) as being unpatentable over Sidwell.

Applicant's independent claim 19 recites "loading a plurality of groups of bits from a source into a plurality of non-contiguous groups of bits of a destination register, and duplicating the plurality of non-contiguous groups of bits in the destination register into subsequent groups of bits in the destination register." In claim 19, the groups of bits duplicated are those that were loaded into non-contiguous locations in the destination register. For example, as explained in page 17, line 20, to page 18, line 19 of the originally filed application, in one situation a source may include four groups, numbered 0-3, arranged in the order of 3/2/1/0 (3 being the most significant group). Claim 19, may be used, for example, to cause groups 3 and 1 to be loaded into groups 2 and 0 of a destination register (assuming, in this example, that the destination register has the same bit-length as the source). Groups 0 and 2 of the destination register are non-contiguous groups. Groups 0 of the destination register is duplicated and stored in group 1 of the destination register. Similarly, group 2 of the destination register is duplicated and the copied value is stored in subsequent group 3 of the destination register. After performance of the method recited in claim 19, the resultant destination register holds the value 3/3/1/1.

The examiner argues, with respect to claim 19, that:

5. Referring to claim 19, Sidwell has taught a method executed in a processor comprising:

a. loading a plurality of groups of bits from a source into a plurality of noncontiguous groups of bits of a destination register (Figure 17, see zip2n4v2p, For the purpose of this rejection, the source is V3/V2/V1/VO, then the zip2n4v2p instruction is performed on the source to produce a destination V2/V2/VO/VO. The bits in source groups VI and VO are loaded into the first location and the third location of the destination memory.); and

b. duplicating the plurality of non-contiguous groups of bits in the destination register into subsequent groups of bits in the destination register (Figure 17, see zip2n4v2p, the V2 bits in the first destination memory location are duplicated into the second destination memory location, and the VO bits in the third destination memory location are duplicated into the fourth destination memory location.).

Applicant disagrees with the examiner's characterization of the zip instructions, particularly with the characterization of the *zip2n4v2p* instruction.

As applicant explained in the Amendment in Reply to the June 15, 2005, Office Action, Sidwell describes instructions that are used for effecting matrix transposition operations (see Abstract). Among the instructions that Sidwell uses to facilitate matrix operations are the zip, unzip and flip instructions that are executed on the twist and zip unit 74 (shown in FIG. 2 and FIGS. 9-11). With reference to the zip (or shuffle) operations, Sidwell explains that "[t]his takes a source string consisting of pairs of object strings and interleaves the objects from the object string pairs to produce a single resultant string of the same length as the source string. This is a perfect shuffle" (page 6, lines 18-20).

A graphical illustration of what the zip (shuffle) instructions do is provided in FIG. 7. For example, the *zip2n4v2p* instruction (as Sidwell explains at page 6, lines 39-41, the 2n4v2p syntax indicates that the operation is performed on 2 source vectors, each vector having 4 elements that are each 16 bits long), places bits in the various source vector elements into designated locations in the destination register. At no point, however, does Sidwell describe that any of the zip, unzip or flip instructions cause any of the bits placed into the destination register to be duplicated.

The examiner relies on FIG. 17 to argue that Sidwell shows loading of groups of bits from the source into a plurality of non-contiguous groups of bits of the destination register, and duplicating the plurality of non-contiguous bits into subsequent groups of bits in the destination

register. However, FIG. 17 clearly shows that the resultant replication of groups of bits in the destination register is performed not by duplicating groups of bits that have been placed in the destination register, but rather by placing a group of bits from the source register directly into two adjacent group locations in the destination register. For example, upon execution of the *zip2n4v2p* instruction, the group of bits V0 in the source register is placed into two sequential bit group locations in the destination register, and the group of bits V1 is placed into two sequential bit group locations in that same destination register.

Indeed, Sidwell explicitly states "[a]nother way of replicating the vector elements is by using sips [*sic*]. Figure 17 shows how this is achieved. The code sequence which does that for matrix multiplication is shown in Annexe A, Sequence (V)" (page 10, lines 56-57). Annexe A, Sequence (V) in turn shows that no replication operation is performed on any of the vectors (source or destination).

FIG. 17 merely shows that resultant replication of bits may be achieved by performing multiple executions of the *zip2n4v2p* instruction on the vector values held in the various source and destination registers, without having to actually duplicate groups of bits. Accordingly, FIG. 17 does not show, and Sidwell does not describe, that groups of bits placed in the destination are duplicated. Sidwell, therefore, does not disclose or suggest at least the feature of "duplicating the plurality of non-contiguous groups of bits in the destination register into subsequent groups of bits in the destination register," as required by applicant's independent claim 19. Thus, applicant's claim 19 is patentable over the cited art.

Applicant's claims 20-23 depend from independent claim 19 and are therefore patentable for at least the same reasons as independent claim 19.

Applicant's independent claims 73, 83, and 88 recites "load a plurality of groups of bits of the source into a plurality of non-contiguous groups of bits in the destination register and duplicate the plurality of non-contiguous groups of bits into subsequent groups of bits in the destination register," or similar language. For reasons similar to those provided with respect to applicant's independent claim 19, at least this feature is not disclosed by the cited art. Therefore, independent claims 73, 83, and 88 are patentable over the cited art.

Claims 74-76 depend from independent claim 73 and are therefore patentable for at least the same reasons as independent claim 73. Claims 84-87 depend from independent claim 83 and

are therefore patentable for at least the same reasons as independent claim 83. Claims 89-92 depend from independent claim 88 and are therefore patentable for at least the same reasons as independent claim 88.

In addition, as noted above, the examiner rejected claims 20, 84 and 89 under 35 U.S.C. §102(b) as being anticipated by Sidwell, and rejected claims 74 and 76 under 35 U.S.C. §103(a) as being unpatentable over Sidwell.

Applicant's claim 20 describes that the source recited in independent claim 19 is an extended multimedia register. Extended multimedia (XMM) registers are special registers that are designed to improve multimedia performance by enabling simultaneous processing of operand values.

The examiner contends that Sidwell has taught that the source is an extended multimedia register, and has pointed to Figure 6, element 104 for support for that contention. Applicant respectfully disagrees.

Sidwell shows, at FIG. 6, byte-replicate logic circuitry that processes source operands (see also Sidwell's page 6, lines 1-2). While the logic circuitry of FIG. 6 includes, as identified by Sidwell's at page 5, line 46, an input buffer 104 to store the source operand, nowhere does Sidwell disclose or suggest that such an input buffer, even if it happens to be a register, is an extended multimedia register, as required by applicant's claim 20. As applicant explained above, because extended multimedia (XMM) registers are configured to enable simultaneous processing of operands, such XMM registers facilitate performance of applicant's method. There is no indication that Sidwell's input buffer 104 could likewise facilitate the performance of applicant's method as recited in the claims. Accordingly, claim 20 is patentable over the cited art.

Applicant's claims 74, 76, 84, and 89 also recite "extended multimedia register." For reasons similar to those provided with respect to applicant's claim 20, at least this feature is not discloses by the cited art. Accordingly, applicant's claims 74, 76, 84, and 89 are patentable over the cited art.

Applicant's claim 21 depends from claim 20 and is therefore patentable for at least the same reasons as claim 20. Applicant's claim 85 depends from claim 84 and is therefore patentable for at least the same reasons as claim 84. Applicant's claim 90 depends from claim 89 and is therefore patentable for at least the same reasons as claim 89.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fees are believed due. Please apply any charges or credits to deposit account 06-1050, referencing attorney docket 10559-644001.

Respectfully submitted,

Date: Dec. 30, 2005

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